BACHELOR OF COMPUTER APPLICATIONS (BCA_NEW)

BCA_NEW ASSIGNMENT SEMESTER-2

ASSIGNMENTS

(January, 2025 & July, 2025 sessions)

FEG-02, MCS-202, MCS-203, MCSL-204, MCS-201, MCSL-205

SCHOOL OF COMPUTER AND INFORMATION SCIENCES , INDIRA GANDHI NATIONAL OPEN UNIVERSITY ,MAIDAN GARHI, NEW DELHI – 110 068

CONTENTS

Important Notes

1. Submit your assignments to the Coordinator of your Study Centre on or before the due date.
2. Assignment submission before due dates is compulsory to become eligible for appearing in corresponding Term End Examinations.
3. To become eligible for appearing in the Term End Practical Examination for the lab courses, it is essential to fulfill the minimum attendance requirements as well as submission of assignments (on or before the due date

Course Code	**:**	**MCS-202**
Course Title	**:**	**Computer Organisation**
Assignment Number	**:**	**BCA_NEW(II)/202/Assignment/2025**
Maximum Marks	**:**	**100**
Weightage	**:**	**25%**
Last Dates for Submission	**:**	**30th April,2025(For January Session)**
		31st October, 2025 (For July session)

There are four questions in this assignment, which carries 80 marks. The remaining 20 marks are for viva voce. You may use illustrations and diagrams to enhance the explanations. Please go through the guidelines regarding assignments given in the Programme Guide for the presentation format. The answer to each part of the question should be confined to about 300 words. Make suitable assumptions, if any.

Question 1(Covers Block1) **(2 marks each × 10 parts =20 Marks)**

(a) Explain the Harvard architecture with the help of a diagram. Explain how the data and instructions will be stored in Harvard Architecture.

(b) Explain how a computer will execute the following high-level language program segment:

```
int a=25, b=75, c;
c=b-a;
```

(c) Perform the following conversion of numbers:

- **(i)** Decimal $(9567438120)_{10}$ to binary and hexadecimal.
- **(ii)** Hexadecimal $(8FAEB1DC)_h$ to binary and Octal.
- **(iii)** ASCII String "ABCabc$#4325 & Unicode" to UTF 8
- **(iv)** Octal $(41302576)_O$to Decimal

(d) Simplify the following function using K-map: F(A, B, C, D) = Σ (0,2, 4, 6, 8, 10, 15). Draw the circuit for the simplified function using NAND gates.

(e) Consider the Adder-Subtractor circuit given in Unit 3 of Block 1. Explain how this circuit will perform subtraction (A-B) if the value of A is 0011 and B is 1101. You must list all the bit values, including C_{in} and C_{out} and overflow condition.

(f) Make the Truth Table and draw the logic diagram of a 4×1multiplexer. Explain its functioning with the help of an example input.

(g) Assume that a source data value 1111 was received at a destination as 0111. Show how Hamming's Error-Correcting code will be appended to the source data, so this one-bit error is identified and corrected at the destination. You may assume that the transmission error occurs in the source data and not in the error correction code.

(h) Explain the functioning of the JK flip-flop with the help of a logic diagram and characteristic table. Also, make and explain the excitation table of this flip-flop.

(i) Explain the functioning of a master-slave flip-flop with the help of a diagram.

(j) Represent $(-126.5)_{10}$ and $(0.015625)_{10}$ in IEEE 754 single precision format.

Question 2(Covers Block 2) **(4 marks each × 5 parts =20 Marks)**

(a) (i) Explain the structure of a 16 × 4 ROM with the help of a diagram.

(ii) How many memory chips of size 64K ×4 bits are needed to build a RAM of size 32 M words if the word size of RAM is16 bits?

(iii) Find the storage capacity of a Magnetic disk with 8 recording surfaces, and 128 tracks consisting of128 sectors each. You may assume that each sector can store 512KB of data.

(iv) Find the rotational latency of a disk that rotates at 3000 rpm.

(b) Consider that the main memory of a computer is 128 words (assume a memory word to be 16 bits). The cache memory of this computer is 8 blocks of size, 32 bits each. Find the cache addresses for the main memory addresses0111001_2 and1010101_2if the following cache mapping schemes is used:

(i) Associative cache mapping

(ii) Direct cache mapping

(iii) Two-way set associative cache mapping

(c) What is the DMA technique of data transfer? Why is DMA needed? Explain the DMA breakpoints in an instruction cycle with the help of a diagram. Also, explain any one DMA configuration.

(d) Explain the Programmed I/O and Interrupt driven I/O techniques with the help of a diagram of each. How are these two techniques different from each other? Also, explain the steps of interrupt processing.

(e) Explain the features of the following I/O Technologies:

(i) Bit-mapped Graphics Image and Frame Buffer

(ii) Refresh Rate of Video controllers

(iii) Impact printers

(iv) Voice-based Input devices

Question 3 (Covers Block 3) **(4 marks each × 5 parts =20 Marks)**

(a) Explain the functioning of Branch, Jump and Bit manipulation instructions with the help of an example/diagram of each. Also, explain the following addressing modes with the help of an example– Relative Addressing Scheme and Base register addressing scheme.

(b) Demonstrate how the size of a machine program changes for the computation of the expression a=(x*y) + (x*y+z) when different instruction sets, having zero address, one address, two address and three address instructions, are used.

(c) Consider a machine that uses PC, IR, AC, and MAR registers to execute different instructions. All the memory accesses during instruction execution bring data to a register named XR. ALU of the machine performs the addition operation using AC and XR registers, and results are stored in the AC register. List and explain all the microoperations required to execute the following machine instructions:

AC ← AC + X; where X is the address of a direct operand in the Memory

Assume that PC is currently pointing to this instruction. Make and state suitable assumptions, if any.

(d) Explain the Wilkes Control unit with the help of a diagram. Also, explain different microinstruction formats with the help of diagrams.

(e) Explain the use of large register files in RISC processors. Also, explain the circular buffer organisation of overlapped register windows in RISC with the help of a diagram.

Question 4(Covers Block 4) **(5 marks each × 4 parts =20 Marks)**

(a) What are the different types of Registers used in the 8086 microprocessor? Explain the use of each type of register of the 8086 microprocessor. Compute the physical address for the following<segment register: offset> pairs in an 8086 microprocessor:

(i) CS: IP = $12FB_h$: $567D_h$
(ii) DS:BX = $99AE_h$: 7551_h
(iii) SS: SP = 3241_h:$77FF_h$

(b) How does the 8086 microprocessor process interrupt? Explain with the help of a diagram. Write a program using 8086 assembly language to output a string: "Present Year is 2025."

(c) Write a program in 8086 assembly language, which converts an input of 4 ASCII digits to an equivalent hexadecimal number. For example, an input string of 4 ASCII digits, say "4", "5", "3", "2," will be converted to the hexadecimal equivalent of number 4532, which is $11B4_h$. Explain the algorithm of the program.

(d) List the characteristics of the following:
(i) Arithmetic Pipeline
(ii) Instruction Pipeline
(iii) SIMD array processor
(iv) Interconnection Structures of Multiprocessors
(v) Cache Coherence